

ABSTRACT OF THE DISCLOSURE**MIXED-MODE HARDWARE MULTITHREADING**

A mixed-mode multithreading processor is provided. In one embodiment, the multi-mode multithreading processor includes a multithreaded register file with a plurality of registers, a thread control unit, and a plurality of hold latches. Each of the hold latches and registers stores data representing a first instruction thread and a second instruction thread. The thread control unit provides thread control signals to each of the hold latches and registers selecting a thread using the data. The thread control unit provides control signals for interleaving multithreading except when a long latency operation is detected in one of the threads. During a predetermined period corresponding approximately to the duration of the long latency operation, the thread control unit places the processor in a mode in which only instructions corresponding to the other thread are read out of the hold latches and registers. Once the predetermined period of time has expired, the processor returns to interleaving multithreading.